REMARKS

Applicant is in receipt of the Office Action mailed March 30, 2004. Claims 1-47 are currently pending in the present case. Reconsideration of the present case is earnestly requested in light of the following remarks.

The Office Action asserts that "claims 1, 8, 15, 23, 30, and 37 are independent claims." Applicant respectfully submits that claims 1, 17, 36, and 37, and 43 are independent claims, and that claims 8, 15, and 30 are dependent claims.

§102 Rejections

Claims 1, 3, 5-11, 13-16, 36, 37, 39-43, 45-47 were rejected under 35 U.S.C. 102(b) as being anticipated by McKaskle et al. (U.S. Pat. No. 5,481,741, hereinafter, "McKaskle"). This rejection is respectfully traversed.

Examiner asserts in the Office Action:

> As per claim 1, McKaskle et al. teaches a method for creating a graphical program which performs register accesses in a hardware device, wherein the method operates in a computer including a display screen and a user input device (col. 5, lines 46-61), the method comprising:
>
> displaying on the screen a register access node in the graphical program in response to user input (fig. 99, col. 49, lines 49-56); and
>
> configuring the register access node to access one or more registers of a hardware device (fig. 99, col. 49, lines 49-56);. . .(*emphasis added*)

As the Examiner is certainly aware, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In the Office Action, Examiner asserts: "Microsoft dictionary defines hardware register to be a set of memory within a microprocessor or other electronic device used to hold data for a particular purpose. Therefore, the shift register taught by Mckaskle [sic] (col. 9, lines 49-56) fits the definition of a hardware register, since it holds data within an electronic device" (*emphasis added*).

As the Examiner is certainly aware, an inventor's practitioner and/or the inventor may be their own lexicographers and grammarians. *W.L. Gore & Associates v. Garlock, Inc.*, 721 F.2d 1540, 1558, 220 USPQ 303, 306 (Fed. Cir. 1983); *Fromson v. Advance Offset Plate, Inc.*, 720 F.2d 1565, 219 USPQ 1137, 1140 (Fed. Cir. 1983); *Autogriro Co. v. U.S.*, 384 F.2d 391, 397, 155 USPQ 697, 702 (Ct. Cl. 1967).

Upon further inspection, McKaskle teaches and discloses:

> Shift Registers
>
> Referring now to FIG. 97, **shift registers** (available for While Loops and For Loops) **are local variables** that transfer values from one iteration to the next. A shift register is created by popping up on the left or right loop border and selecting Add Shift Register from the pop-up menu.
>
> As shown in FIG. 97, the shift register contains a pair of terminals directly opposite each other on the vertical sides of the loop border. The right terminal stores the data upon the completion of an iteration. That data is shifted at the end of the iteration and it appears in the left terminal at the beginning of the next iteration (see FIG. 98). A **shift register** can hold any data type--numeric, Boolean, string, array, and so on. The shift register automatically adapts to the data type of the first object that is wired to the shift register.
>
> As shown in FIG. 99, the shift register can be configured to remember values from several previous iterations. This feature is very useful when averaging data points. Additional terminals are created to access values from previous iterations by popping up on the left terminal and choosing Add Element from the pop-up menu. For example, if three

elements are added to the left terminal, values can be accessed from the last three iterations. (McKaskle col. 49, lines 33-56) (*emphasis added*)

Thus, the term "shift register" as used in McKaskle is "a local variable" in a graphical program.

Thus, Applicant respectfully submits that McKaskle's shift register is specifically *not* a hardware register of a device, but rather, is simply a software variable.

In contrast, Applicant's invention as currently recited in claim 1 includes in pertinent part, ". . .configuring the register access node to access one or more registers of the hardware device, wherein said configuring includes accessing a description of the hardware device for information regarding the one or more registers of the hardware device. . ." (*emphasis added*). McKaskle nowhere teaches or suggests this feature.

Accordingly, Applicant respectfully submits that, at least for the reasons presented, claim 1 is patentably distinguished over McKaskle, and claim 1 and those claims dependent therefrom are allowable.

In contradistinction to McKaskle, Applicant's invention as currently recited in claim 36 includes in pertinent part, ". . . wherein the register access node is operable to access the selected registers of the hardware device during execution of the graphical program" (*emphasis added*). McKaskle nowhere teaches or suggests this feature.

In further contradistinction to McKakle, Applicant's invention as currently recited in claim 36 includes in pertinent part, ". . .connecting an input of the register access node to receive the description of the hardware device in response to user input. . ." McKaskle nowhere teaches or suggests this feature.

Accordingly, Applicant respectfully submits that, at least for the reason or reasons presented, claim 36 is patentably distinguished over McKaskle, and claim 36 is allowable.

Contrary to McKaskle, Applicant's invention as currently recited in claim 37 includes in pertinent part, ". . .configure the register access node to access one or more registers of the hardware device, wherein, in configuring the register access node to

access the one or more registers of the hardware device, the program instructions are executable by the processor to access a description of the hardware device for information regarding the one or more registers of the hardware device. . ." (*emphasis added*). McKaskle nowhere teaches or suggests this feature.

Accordingly, Applicant respectfully submits that, at least for the reasons presented, claim 37 is patentably distinguished over McKaskle, and claim 37 and those claims dependent therefrom are allowable.

In contrast to McKaskle, Applicant's invention as currently recited in claim 43 includes in pertinent part, ". . .configure the register access node to access one or more registers of the hardware device, wherein, in configuring the register access node to access the one or more registers of the hardware device, the processor is operable to execute the program instructions to access a description of the hardware device for information regarding the one or more registers of the hardware device. . ." McKaskle nowhere teaches or suggests this feature.

Accordingly, Applicant respectfully submits that, at least for the reasons presented, claim 43 is patentably distinguished over McKaskle, and claim 43 and those claims dependent therefrom are allowable.

Removal of the §102 rejections of claims 1, 3, 5-11, 13-16, 36, 37, 39-43, 45-47 is respectfully requested.

§103 Rejections

The Office Action cites various of the dependent claims as being rejected under 35 U.S.C. 103. Independent claims 1, 36, 37, and 43 have been amended to overcome rejections under 35 U.S.C. 102. Applicant respectfully submits that amended independent claims 1, 36, 37, and 43 are nonobvious and are allowable, as well. Applicant respectfully submits: "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine* , 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)" as stated in the MPEP §2143.03. With this in mind, Applicant respectfully submits that claims 1-16, and 36-47 are allowable.

As held by the U.S. Court of Appeals for the Federal Circuit in Ecolochem Inc. v. Southern California Edison Co., an obviousness claim that lacks evidence of a suggestion or motivation for one of skill in the art to combine prior art references to produce the claimed invention is defective as hindsight analysis.

In addition, the showing of a suggestion, teaching, or motivation to combine prior teachings "must be clear and particular . . .. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'." *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). The art must fairly teach or suggest to one to make the specific combination as claimed. That one achieves an improved result by making such a combination is no more than hindsight without an initial suggestion to make the combination.

Claims 2, 38, and 44 were rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle in view of Sojoodi et al. (U.S. Pat. No. 5,847,953, hereinafter, "Sojoodi"). This rejection is respectfully traversed.

Applicant submits that neither McKaskle nor Sojoodi provides a motivation to combine the teaching(s) of McKaskle and Sojoodi to produce Applicant's invention as represented in claim 2, 38, and 44, and so combining McKaskle and Sojoodi is improper. Moreover, even if McKaskle and Sojoodi were properly combinable, which Applicant argues they are not, the resulting combination would not produce Applicant's invention as claimed.

For example, in addition to the features and limitations of the independent claims, Applicant submits that neither McKaskle nor Sojoodi teaches the limitations, "displaying a list of registers, and receiving user input to select one or more of the registers from the list of registers."

The Examiner cites Sojoodi col. 17, lines 18-46 in asserting that Sojoodi teaches these limitations. Applicant notes that Sojoodi states: "The reader is referred to FIG. 7

for an explanation of the error in input terminal" (Sojoodi col. 16, lines 63-65) (*emphasis added*), and that Sojoodi col. 17, lines 18-46 recites in part:

> Referring now to FIG. 7, a screen shot including a help screen illustrating the terminals of a VISA Write function node is shown. The VISA write node is illustrative of most VISA function nodes in that nodes of the present invention and enable the VISA nodes to be wired together such that the VISA session identifier and error status associated with the performance of VISA operations to be propagated through the various nodes comprising the VI. This feature advantageously enables, inter alia, type propagation checking and class propagation. This feature further provides the code generation method of each VISA node with the VISA session identifier required as an input parameter to the VISA library functions.it has a VISA session input terminal, a dup VISA session output terminal, an error in input terminal, and an error out output terminal. These four terminals are advantageously provided on the VISA. (Sojoodi col. 17, lines 18-46) (*emphasis added*)

Thus, Sojoodi teaches terminals of a VISA Write function in a graphical program in col. 17, lines 18-46, and FIG. 7 does not show a single register or a list of registers.

As Examiner is certainly aware, "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations" as stated in the MPEP §2143 (*emphasis added*).

Applicant respectfully submits that combining a local variable from McKaskle with a VISA Write function in a graphical program from Sojoodi does not teach or suggest all the claim limitations of claims 2, 38, or 44.

For example, Applicant submits that combining a local variable from McKaskle with a VISA Write function in a graphical program from Sojoodi does not teach or

suggest ". . .receiving user input to select one or more of the registers from the list of registers" (*emphasis added*) as recited in pertinent part by claim 2. Accordingly, Applicant respectfully submits a *prima facie* case of obviousness has not been established to reject claim 2. Thus, Applicant respectfully submits that claim 2 is allowable for at least this further reason.

> Sojoodi further teaches and discloses:
>
> Referring now to FIG. 9c, a user may choose from a number of VISA operations to drop on the block diagram from the VISA functions palette. In the embodiment shown, a Find Resource function node, an Open function node, a Close function node, a Read function node, a Write function node, a Clear device function node, a Read Service Request Status (from a message based device) function node, an Assert Trigger function node, a Lock device function node, a Lock Asynchronous function node, an Unlock device function node, a VISA attribute node, a Status Description function node, and pull-right menus for VISA events, VISA High-Level Register Access and VISA Low-Level Register Access function nodes are provided. The reader is referred to the VISA Library Reference chapter of the LabVIEW Instrument I/O VI Reference Manual, which is hereby incorporated by reference, for more detail about each of the VISA nodes. Most of the nodes correspond to VISA I/O Library 52 functions, as described previously with regard to the VISA Open, Write and Read function nodes and their relationship to the viOpen(), viWrite() and viRead() routines, respectively. Most VISA nodes will accept VISA refnums of all classes although a particular function, or method, may be valid only for a subset of classes. An example is VISA Poke 16 which is defined only for VXI/GPIB-VXI MBD and VXI/GPIB-VXI RBD classes. (Sojoodi col. 18, lines 14-38) (*emphasis added*)

Applicant has submitted the LabVIEW Instrument I/O VI Reference Manual in an Information Disclosure Statement accompanying this Present Amendment.

The LabVIEW Instrument I/O VI Reference Manual on page 4-15 describes the ability of the user to: "5. Edit the block diagram. . .c. Change the constants labeled **register offset** to be the registers that you plan to peek or poke. Add or remove the VISA Peek 16 function or the VISA Poke function 16, as necessary. . ."

Applicant submits that per the above description from the LabVIEW Instrument I/O VI Reference Manual, Sojoodi in combination with McKaskle (and/or the LabVIEW Instrument I/O VI Reference Manual) does not teach or disclose all of the features and limitations of independent claim 2. Accordingly, Applicant respectfully submits that claim 2 is patentably distinguished and non-obvious over McKaskle and Sojoodi, taken both singly and in combination, and is thus allowable.

Claims 38 and 44 include similar limitations as claim 2, and so the above arguments apply with equal force to these claims. Thus, for at least the reasons provided above, Applicant submits that claims 38 and 44 are patentable distinct and unobvious over McKaskle and Sojoodi, and are thus similarly allowable.

Applicant respectfully requests removal of the 103 rejection of claims 2, 38, and 44.

Claims 4, 12, 17, 18, 23-25, 29, and 30-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle in view of Yamamoto et al. This rejection is respectfully traversed.

In the Office Action, Examiner cited U.S. Pat. No. 5,847,953 to Yamamoto et al. However, U.S. Pat. No. 5,847,953 is by Sojoodi. The Notice of References Cited includes U.S. Pat. No. 6,553,431 to Yamamoto et al. For a purpose of expediting prosecution, Applicant shall assume Yamamoto et al. to be U.S. Pat. No. 6,553,431.

The Office Action cites various of the dependent claims as being rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle in view of Yamamoto et al. Independent claims 1, 36, 37, and 43 have been shown above to be allowable, and thus claims respectively dependent thereon are similarly allowable for at least the reasons provided above. Applicant respectfully submits that claims 4, 12, 17, 18, 23-25, 29, and

30-35 are patentably distinguished and non-obvious over McKaskle in view of Yamamoto, and are thus allowable.

Moreover, Applicant submits that neither McKaskle nor Yamamoto provides a motivation to combine the teaching(s) of Yamamoto and McKaskle to produce Applicant's invention as represented by claims 4, 12, 17, 18, 23-25, 29, and 30-35, and so the alleged combination of McKaskle and Yamamoto is improper. Furthermore, Applicant submits that even if McKaskle and Yamamoto were properly combinable, which Applicant argues they are not, the resulting combination would not produce Applicant invention as represented by claims 4, 12, 17, 18, 23-25, 29, and 30-35.

For example, as noted above, McKaskle teaches and discloses that a "shift register" is "a local variable" in a graphical program (McKaskle col. 49, lines 33-56).

In the Office Action, Examiner admits: "However, McKaskle et al. fails to teach the program wherein the register node receives the description, wherein the register access node is operable to access registers of the hardware device during the execution of the graphical program." Applicant submits that Yamamoto fails to overcome this deficiency of McKaskle.

Yamamoto teaches and discloses:

> Subsequently, in the step S15, an output-side device profile acquirement demand instruction to demand to acquire the device profile of the output device is transmitted to the file server 5 through the LAN 6. Then it is judged in a step S16 whether or not the file server 5 responds to the instruction in a certain time. If judged that the server 5 responds, the flow advances to a subsequent step S17 to search for the output-side device profile capable of performing data output in the acquired output-side device profiles, on the basis of the contents of the acquired input-side device profile. That is, it is judged whether or not the output device which has the output-side device profile of which transfer protocol and data

format are coincident with those of the input-side device profile exists. (Yamamoto et al. col. 10, lines 12-25) (*emphasis added*)

In other words, Yamamoto et al. teach and disclose judging whether or not an output device can make use of data from an input device. Yamamoto et al. does not teach or suggest accessing registers. Furthermore, Yamamoto et al. does not teach or suggest accessing registers of either the input device or the output device.

In contradistinction to McKaskle and/or Yamamoto et al., Applicant's invention as currently recited in claim 17 includes in pertinent part, ". . . displaying on the screen a register access node in response to user input, wherein the register access node is operable to access the hardware device. . ." (*emphasis added*). McKaskle and/or Yamamoto et al. nowhere teach or suggest this feature. Applicant respectfully submits that, at least for the reasons presented, claim 17 is patentably distinguished over both McKaskle and Yamamoto et al., taken both singly and in combination.

Additionally, in contrast to Yamamoto et al., claim 17 includes in pertinent part, ". . .wherein the register access node receives the description, wherein the register access node is operable to access registers of the hardware device during execution of the graphical program based on the description of the hardware device." Yamamoto nowhere teaches or suggests this feature.

Applicant thus respectfully submits that claim 17 is patentably distinguished over both McKaskle and Yamamoto et al., taken both singly and in combination. Accordingly, Applicant respectfully submits that, at least for the reason or reasons presented, claim 17 and those dependent therefrom are patentably distinct and non-obvious over McKaskle and Yamamoto, and are thus allowable.

Claims 19-22, and 26-28 were rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle in view of Yamamoto et al. further in view of McIntyre et al. (U.S. Pat. No. 6,229,538, hereinafter, "McIntyre"). This rejection is respectfully traversed.

The Office Action cites various of the dependent claims as being rejected under 35 U.S.C. 103(a) as being unpatentable over McKaskle in view of Yamamoto et al. further in view of McIntyre. Independent claims 1, 36, 37, and 43 have been shown above to be allowable, and thus claims respectively dependent thereon are similarly allowable, for at least the reasons provided above.

Moreover, neither McKaskle, Yamamoto, nor McIntyre provides a motivation to combine the teaching(s) of McKaskle, Yamamoto, and McIntyre to produce Applicant's invention as claimed, and so the combination is improper. Furthermore, Applicant submits that even if McKaskle, Yamamoto, and McIntyre and were properly combinable, which Applicant argues they are not, the resulting combination would not produce Applicant invention as represented by claims 19-22, and 26-28.

For example, in the Office Action, the Examiner asserts with regards to claim 19 that McIntyre teaches: "receiving user input to select one or more of the registers from the list of registers ([McIntyre] Fig 5, col. 8, lines 38-64)."

However, Applicant notes that McIntyre actually teaches and discloses:

> FIG. 5 is a block diagram illustrating one embodiment in which the intermediate driver 310 defines a Heartbeat Multicast Address (HMC) and where the intermediate driver 310 causes each NIC team member to register the HMC address. Upon power-up, boot or initialization, the O/S 301 starts each of the NIC drivers D1-D4 and the intermediate driver 310. The intermediate driver 310 detects and collects any and all multicast addresses (not shown) supported by each supported higher level protocol, such as the TCP/IP 302, IPX 304 and NetBEUI 306, and appends its own multicast address(es), which includes the HMC address. The intermediate driver 310 then requests that each NIC driver D1-D4 register the list of multicast addresses, including the HMC address. As shown in FIG. 5, each NIC driver D1-D4 and the corresponding NICs N1-N4 are programmed to detect the single node address A and the HMC address. It is noted that although only the HMC address is shown, each NIC driver D1-D4 may be programmed with a table of multicast addresses. The intermediate driver

> 310 also includes heartbeat logic 502 that includes memory for storing the HMC address and a status table 504 that maintains the status of each of the ports P1-P4 (including the NIC drivers D1-D4 and the NICs N1-N4) of the team. The intermediate driver 310 also includes a timer or timer logic 506 that determines the heartbeat period for checking the status of the ports P1-P4. The heartbeat period is referred to as the HEARTBEAT_TIMER_SPEED. (McIntyre col. 8, lines 37-64) (*emphasis added*)

Applicant respectfully submits that McIntyre uses the word "register" as a verb. In other words, "The intermediate driver 310 then requests that each NIC driver D1-D4 register the list of multicast addresses, including the HMC address" (McIntyre col. 8, lines 47-50) (*emphasis added*), could be written "The intermediate driver 310 then requests that each NIC driver D1-D4 enlist the list of multicast addresses, including the HMC address."

Furthermore, claim 19 recites: "The method of claim 18, wherein said configuring the register access node includes: displaying a list of registers described in the description of the hardware device; receiving user input to select one or more of the registers from the list of registers" (*emphasis added*). McKaskle, Yamamoto et al., and/or McIntyre nowhere teach or suggest this feature. Thus, Applicant respectfully submits claim 19 is allowable for at least this further reason.

In the Office Action, the Examiner asserts with regards to claim 26: "selecting a first register from said list of registers;. . .repeating the above steps for one or more registers of the hardware device ([McIntyre] Fig 5, items d1-4, col. 8, lines 37-64)."

Applicant respectfully submits that items D1-D4 are drivers or software for using NICs (Network Interface Cards) with a computer system and are not registers of a hardware device. "As shown in FIG. 3, four NIC [Network Interface Card] drivers D1-D4 are installed on the computer system 100, each for supporting and enabling communications with a respective port of one of the NICs [Network Interface Cards] N1-N4" (McIntyre col. 5, lines 54-57) (*emphasis added*).

Further, claim 26 recites: "The method of claim 17, wherein receiving user input further comprises: selecting a first register from said list of registers; associating a first terminal of the register access node with said first register; selecting the first terminal as a read or a write terminal; connecting the first terminal to a node in the graphical program; and repeating the above steps for one or more registers of the hardware device" (*emphasis added*). McKaskle, Yamamoto et al., and/or McIntyre nowhere teach or suggest this feature. Thus, Applicant respectfully submits claim 26 is allowable for at least this further reason.

Thus, Applicant submits that claims 19 and 26, and claims respectively dependent thereon, are patentably distinct and non-obvious over McKaskle in view of Yamamoto et al., and further in view of McIntyre, and are thus allowable for at least the reasons provided above.

Removal of the §103 rejections of claims 2, 4, 12, 17-35, 38, and 44 is respectfully requested.

Applicant also respectfully submits that numerous ones of the dependent claims recited further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-38200/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

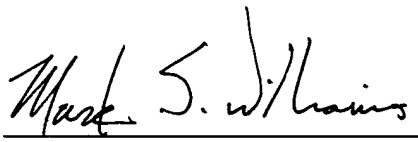
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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